REMARKS/ARGUMENTS

The present application provides a method, apparatus and program product for a self-healing, reconfigurable logic emulation system, wherein if a signal wire becomes faulty in an emulation cable during an emulation run, the runtime software can automatically reconfigure the emulator to reroute the data destined for the faulty signal wire across a spare wire. Such a feature enables a user to restart the emulation run without having to recompile the simulation model to account for the hardware fault.

Reconsideration of the application, as amended, is requested. No claims have been amended in this response, thus no new matter has been added. Claims 1-16 remain pending in this application.

In section 6 of the Office Action, the Examiner rejects claims 9, 10, 12-14, and 16 under 35 U.S.C. §102(b) as being anticipated by Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001. Applicants respectfully traverse this rejection.

The Yu reference cited by the Examiner describes a real time computing system (e.g., fly-by-wire system, navigation system, etc.) where failures can result in data corruption and lower performance, leading to catastrophic failures (Yu, Abstract). Yu proposes several fault tolerant design techniques to be utilized within such real-time computing systems, such as the use of Field-Programmable Gate Arrays (FPGAs), to design more reliable real-time computing systems.

One of the key features of the Yu reference is that the design of the real-time computer system is re-configurable. For example, on page 6, third paragraph, Yu states that "Our scheme configures the original design into another fault tolerant design that has smaller area, so the damaged element can be avoided".

With respect to claims 9, 10, 12-14, and 16, the Examiner states that Yu discloses a method for the automatic reconfiguration of faulty signal wires in a logic simulation hardware emulator. Applicants respectfully submit that Yu neither discloses nor suggests a logic simulation hardware emulator, as stated by the Examiner. In the second paragraph of the Yu Abstract on page iv, Yu states that the design described throughout the dissertation is for a robot controller, not for a logic simulation hardware emulator, as provided by the present invention. More specifically, the Yu abstract states:

> "To demonstrate the effectiveness of our design techniques, we implemented a robot control algorithm on FPGAs. Various fault tolerance features are implemented in the robot controller to ensure reliability. Our implementation results show that the performance of the FPGA-based controller with triple modular redundancy (TMR) is comparable to that of a software-implemented control algorithm (with TMR) in a microprocessor, while providing comparable degrees of fault tolerance."

Similarly, the only other examples of real-time computing systems specifically enumerated by Yu are fly-by-wire and navigation systems, neither of which remotely discloses nor suggests a logic simulation hardware emulator.

In fact, Applicants submit that real-time computing systems (such as described in the Yu dissertation) actually teach away from logic simulation hardware emulators, since the simulation emulators inherently function slower than the actual designs they are meant to emulate. Logic simulators/emulators typically function at speeds which are typically orders of magnitude slower than the speeds of the actual hardware they are emulating, and thus nowhere near real-time. In the case of the present invention, the simulation occurs roughly 10-100 times slower than the real time operating speed of the actual hardware emulated.

For these reasons, Applicants respectfully submit that Yu does not provide the necessary claim element of a "logic simulation hardware emulator" as present in claims 9, 10, 12-14, and 16 of the present invention.

In section 8 of the Office Action, the Examiner rejects claims 1-6, 11, and 15 under 35 U.S.C. §103(a) as being unpatentable over Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001, in view of Babb et al., "Logic Emulation with Virtual Wires," published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol., 16, No. 6, June 1997. Applicants respectfully traverse this rejection.

With regard to claim 1, the Examiner states that Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors. Applicants respectfully submit that what is disclosed on page 88-89 and in Table I of Yu, are results when the robot control system employed within the Yu real time computer was emulated by an external simulation system (i.e., Quickturn's System Realizer) in order to verify its functionality. The simulated square wave responses cited by the Examiner are actually generated by the external Cadence Quickturn emulation system, and are not in any way generated by the real-time computer system of Yu itself.

Also, with regard to claim 1, the Examiner states that Yu does not disclose expressly the emulation processors being embodied in a simulation model, or the runtime control program controlling the simulation model. The Examiner goes on to state that the emulation processors as disclosed in Yu are actually FPGAs and that Babb discloses the simulation of interconnected FPGA chips based on a simulation model.

Applicants respectfully submit that the present invention neither discloses nor suggests the use of FPGAs, as described in the Yu and Babb references, so the fact that both references cited by the Examiner use FPGAs is not applicable. While the Applicants agree with the Examiner that the Babb reference does indeed describe a logic simulation hardware emulator, Applicants submit that the real-time computer system described by Yu has nothing to do with logic simulation or hardware emulation, and in fact, Yu teaches away from simulation/emulation since systems such as Babb and the present invention are inherently not real-time (i.e., the

simulators perform the simulation and speeds orders of magnitude less than the real time speed of the hardware being simulated/emulated). Thus, Applicants respectfully submit that there is no motivation to combine the non-real time simulator/emulator reference of Babb with the real-time computing system reference of Yu.

For these reasons, Applicants respectfully submit that claim 1 of the present invention is non-obvious with respect to Yu in light of Babb, and should be in condition for allowance.

Applicants further submit that claims 2-6 depend, either directly or indirectly, from claim 1, which for reasons stated above, is now submitted as being in condition for allowance. Thus, Applicants submit that claims 2-6 are also now in condition for allowance, and should be passed to issuance.

With regard to claim 11, the Examiner states that Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors. Applicants respectfully submit that what is disclosed on page 88-89 and in Table I of Yu, are results when the robot control system employed within the Yu real time computer was emulated by an external simulation system (i.e., Quickturn's System Realizer) in order to verify its functionality. The simulated square wave responses cited by the Examiner are actually generated by the external Cadence Quickturn emulation system, and are not in any way generated by the real-time computer system of Yu itself.

Also, with regard to claim 11, Applicants respectfully submit that the present invention neither discloses nor suggests the use of FPGAs, as described in the Yu and Babb references, so the fact that both references cited by the Examiner use FPGAs is irrelevant. While the Applicants agree with the Examiner that the Babb reference does indeed describe a logic simulation hardware emulator, Applicants submit that the real-time computer system described by Yu has nothing to do with logic simulation or hardware emulation, and in fact Yu teaches away from simulation/emulation since systems such as Babb and the present invention are

inherently not real-time (i.e., the simulators perform the simulation and speeds orders of magnitude less than the real time speed of the hardware being simulated/emulated). Thus, Applicants respectfully submit that there is no motivation to combine the non-real time simulator/emulator reference of Babb with the real-time computing system reference of Yu.

For these reasons, Applicants respectfully submit that claim 11 of the present invention is non-obvious with respect to Yu in light of Babb, and should be in condition for allowance.

With regard to claim 15, the Examiner states that Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors. Applicants respectfully submit that what is disclosed on page 88-89 and in Table I of Yu, are results when the robot control system employed within the Yu real time computer was emulated by an external simulation system (i.e., Quickturn's System Realizer) in order to verify its functionality. The simulated square wave responses cited by the Examiner are actually generated by the external Cadence Quickturn emulation system, and are not in any way generated by the real-time computer system of Yu itself.

Also, with regard to claim 15, Applicants respectfully submit that the present invention neither discloses nor suggests the use of FPGAs, as described in the Yu and Babb references, so the fact that both references cited by the Examiner use FPGAs is not relevant. While the Applicants agree with the Examiner that the Babb reference does indeed describe a logic simulation hardware emulator, Applicants submit that the real-time computer system described by Yu has nothing to do with logic simulation or hardware emulation, and in fact Yu teaches away from simulation/emulation since systems such as Babb and the present invention are inherently not real-time (i.e., the simulators perform the simulation and speeds orders of magnitude less than the real time speed of the hardware being simulated/emulated). Thus, Applicants respectfully submit that there is no motivation to combine the non-real time simulator/emulator reference of Babb with the real-time computing system reference of Yu.

For these reasons, Applicants respectfully submit that claim 15 of the present invention is non-obvious with respect to Yu in light of Babb, and should be in condition for allowance.

In section 9 of the Office Action, the Examiner rejects claims 7-8 under 35 U.S.C. §103(a) as being unpatentable over Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001, in view of Babb et al., "Logic Emulation with Virtual Wires," published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol., 16, No. 6, June 1997, and further in view of Rush, US Patent No. 5,742,181. Applicants respectfully traverse this rejection.

With regard to claims 7 and 8, Applicants respectfully submit that the present invention neither discloses nor suggests the use of FPGAs, as described in the Yu, Babb and Rush references, so the fact that all three references cited by the Examiner use FPGAs is not relevant.

While the Applicants agree with the Examiner that the Babb reference does indeed describe a logic simulation hardware emulator, Applicants submit that the real-time computer system described by Yu has nothing to do with logic simulation or hardware emulation, and in fact Yu teaches away from simulation/emulation since systems such as Babb and the present invention are inherently not real-time (i.e., the simulators perform the simulation and speeds orders of magnitude less than the real time speed of the hardware being simulated/emulated). Thus, Applicants respectfully submit that there is no motivation to combine the non-real time simulator/emulator reference of Babb with the real-time computing system reference of Yu. Applicants respectfully submit that the introduction of yet a third reference, Rush, which discloses an FPGA interconnect architecture that incorporates multiplexers for FPGA selection is irrelevant since the present invention neither discloses nor suggests the use of FPGAs.

In view of the foregoing comments and amendments, the Applicants respectfully submit that all of the pending claims (i.e., claims 1-16) are in condition for allowance and that the application should be passed to issue. The Examiner is urged to call the undersigned at the

below-listed telephone number if, in the Examiner's opinion, such a phone conference would expedite or aid in the prosecution of this application.

CERTIFICATE OF ELECTRONIC TRANSMISSION

I hereby certify that this correspondence and any enclosures are being electronically transmitted via EFS-WEB on the date indicated below.

January 9, 2007
(Date)

Debra A. Peterson
Debra A. Peterson

Respectfully submitted,

By: James R. Nock
James R. Nock, Attorney
Attorney Reg. No.: 42,937
IBM Corporation, Dept 917
3605 Highway 52 North
Rochester, MN 55901-7829
Telephone: (507) 253-4661